

# STORAGE VISIONS® 2018

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AN ENTERTAINMENT STORAGE ALLIANCE™ EVENT



**Danny Sabour, VP of Marketing, Avalanche Technology**

## **TITLE**

**How AI and ML are driving architecture changes**

## **ABSTRACT**

This presentation will discuss the next evolutionary step in memory architectures, technology and what triggers a breakthrough technology enabling new transformational applications. New applications demand higher densities of non-volatile high performance memories at lower power, and lower cost. New Machine learning/AI applications demand server class memory at the compute edge server as well as the end IoT nodes.

Today, NVMe fabric is addressing the I/O performance. Compute is accelerating by dividing the task between the cloud, the edge and the node. Memory subsystems are being matched to the compute engines by supplementing them with the next level of caches such as persistent memory DIMMs as well as non-volatile memories performing as DRAM. This session will present how a new class non-volatile DRAM will enable new use cases in storage, IoT and compute.

## **BIOGRAPHY**

Danny Sabour is the VP of Marketing at Avalanche Technology. He has held various management and executive positions in companies such as Intel, Spansion and Cypress Semiconductor. At Avalanche he drives the future technology roadmap, development and Memory architectures with the next generation of standalone and embedded MRAM. Mr Sabour has over 30 years of experience in the semiconductor industry. His expertise span system-on-chip, flash storage, Non-volatile memories, RAID disk controller arrays and unique controller designs to get the most out of memory devices. Mr Sabour holds a M.Sc. in Computer Science and Electronic Engineering from University College London.

Avalanche Technology is a private semiconductor company headquartered in Fremont, California, United States. The company develops, manufactures and licenses Spin Transfer Torque Magnetic RAM (STT-MRAM). Its proprietary non-volatile memory leverages perpendicular Magnetic Tunnel Junction (pMTJ) cell structure, manufactured on a 300mm standard CMOS process.